

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: HONMURA, et al.
Serial No.: Not yet assigned
Filed: June 26, 2003
For: SEMICONDUCTOR INTEGRATED CIRCUITS

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97 & 1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

June 26, 2003

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

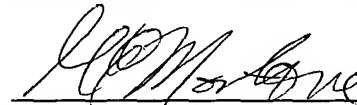
Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (Case: 501.42810X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS LLP



Gregory E. Montone
Registration No. 28,141

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Attachments

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 501.42810X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT HONMURA, Tetsuroo	
		FILING DATE June 26, 2003	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
	AA					
	AB					
	AC					
	AD					
	AE					
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	AG					
	AH					
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	AK					
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FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	AM						
	AN						
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AU	M. Morris Mano, "Logic and Computer Design Fundamental", 2000, Prentice Hall, Chapter 11/Input-Output and Communication, 11-3/I/O Interfaces, Pgs. 580-609
	AV	
	AW	
	AX	
	AY	
	AZ	
Examiner		Date Considered